REMARKS

The claims are claims 1 to 4, 16, 17 and 27 to 54.

Claims 1 to 4, 16, 17 and 27 to 54 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The OFFICE ACTION states that the "plurality of terminals" recited in claims 1, 16 and 27 is indefinite because "there are no claimed meets and bounds of the number of terminals present."

The Applicants respectfully submit that the phrase "plurality of terminals" is particular and definite as required by 35 U.S.C. 112. The OFFICE ACTION states that the invention "would be trivial if there is zero or infinite number of terminals." The Applicants understand that the Examiner objects to the breadth of the "plurality of terminals" limitation. The Applicants agree that this limitation does not exclude much subject matter. However, this limitation does permit unambiguous determination of whether a particular selected number of terminals is within this limitation or not. Namely, provision of zero terminals or of a single terminal is not within the recited "plurality of terminals." Other numbers of terminals are within the recited "plurality of terminals." Thus this limitation is definite because there is no ambiguity whether it is satisfied or not. This "plurality of terminals" is thus a broad but definite limitation. Accordingly, claims 1, 16 and 27 are proper under 35 U.S.C. 112.

Claim 1 to 4, 30, 31 and 37 to 42 were rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The OFFICE ACTION states that method claim 1 does not recite a tangible result to the preamble disclosing "exporting emulation information from the data processor" as the last step outputs the second sequence of second

information blocks, but that information is not tangibly stored in any location once derived from the first information block. Hence, there is no indication there the results of outputting step are tangible.

Claim 1 is amended to recite "a data processor integrated circuit" and that the output is "from the data processor integrated circuit." By these amendments the claim is limited to a particular, tangible result. Accordingly, claims 1 to 4, 30, 31 and 37 to 42 are statutory subject matter.

Claims 30 and 31 recite tangible structure for implementing the claimed method that makes these claims statutory subject matter under 35 U.S.C. 101. Claims 30 and 31 recite "storing a current first information block in a current packet register." This current packet register is a physical structure, thus this is statutory subject matter. Claim 31 further recites "storing the current first information block in a last packet register." This last packet register is a physical structure, thus this is statutory subject matter. Accordingly, claims 30 and 31 are statutory subject matter.

Claims 1 to 4, 16, 17, 27 to 29, 34, 37 to 39, 43 to 45 and 49 to 51 were rejected under 35 U.S.C. 102(e) as being anticipated by Edwards, U.S. Patent No 6,732,307.

Claims 1, 16 and 27 recite subject matter not anticipated by Edwards. Claim 1 recites "collecting internal emulation information from a data processor at a data processor clock rate" and "outputting a sequence of the second information blocks via a plurality of terminals at a transmission clock rate, said first fixed size, said data processor clock rate, said second fixed size and said transmission clock rate related whereby a bit rate of first information blocks equals a bit rate of said second information blocks." Claims 16 and 27 each recite similar limitations. This subject matter is disclosed in the application

at page 38, lines 5 to 12. Edwards fails to disclose the recited relationship between the data sizes and the respective clock rates. The recited "internal information form a data processor at a data processor clock rate" corresponds to trace data bus 221 illustrated in Figure 2 of Edwards. Edwards states at column 8, lines 1 to 7:

> "A trace data bus 221 connects the processor 102 to debug circuit 103 may be capable of transferring information about processor states every processor clock cycle. Also, trace data bus 221 can contain individual bits for each processor state monitored such that multiple states may be monitored within the same clock cycle."

The recited first fixed size is the bus width of trace data bus 221 and the recited data processor clock rate is the processor clock cycle. The only output "via a plurality of output terminals" taught in Edwards is the output of transmission circuit 215 to external system 106. Edwards states at column 7, lines 32 to 39:

> "FIFO 202 holds trace messages awaiting to be sent to an external system 106, or which are waiting to be written into a trace buffer configured in system memory. Destination selector 213 may be programmable to send information to an external system via transmission circuit 215, or save memory in trace buffer (not shown) through memory circuit 214."

Edwards states at column 9, line 65 to column 10, line 1:

> "At step 407, debug circuit 103 may transmit trace messages to an external system, such as through transmission circuit 215 or may store trace messages through a memory circuit 214."

Edwards states at column 10, lines 46 to 51:

> "When matched, a controller associated with the watchpoint channel may provide a signal to debug circuit 103 through communication link 215. This signal may take the form

of state bits indicating particular watchpoint channel states within the processor 102 communicated to debug circuit 103."

Edwards states at column 20, lines 26 to 33:

> "Also, a reference message may be sent to external system 106 during continuous idle periods greater than a predetermined number of time intervals. For example, a predetermined time interval may be 256 time intervals. That is, if a transmission circuit 215 has been idle for more than 256 intervals prior to sending a trace message, a reference message may be inserted into FIFO 202 before the next trace message."

These are the only mentions of transmission circuit 215 in Edwards. None of these portions of Edwards include any mention of the claimed "second information blocks having a second fixed size which differs from the first fixed size of the first information blocks" nor of the claimed "transmission clock rate." Thus Edwards cannot anticipate the limitation that "said second fixed size and said transmission clock rate related whereby a bit rate of first information blocks equals a bit rate of said second information blocks." The limitations of independent claims 1, 16 and 27 related only to the first fixed size of the first information blocks and the data processor clock rate and the second fixed size of the second information blocks at the transmission clock rates. The Examiners citations to the teachings of Edwards regarding trace buffer 227 and FIFO 202 are not relevant to these limitations of claims 1, 16 and 27. Accordingly, claims 1, 16 and 27 are allowable over Edwards.

Claims 2, 17 and 34 recite subject matter not anticipated by Edwards. Claims 27, 17 and 34 each recite "said second fixed size is smaller in size than said first fixed size." The OFFICE ACTION cites Table 8/7 on column 20 as anticipating this subject matter. Edwards states at column 20, lines 26 to 28:

> "Also, a reference message may be sent to external system 106 during continuous idle periods greater than a predetermined number of time intervals."

This teaching of Edwards makes clear that Table 8/7 cited in the OFFICE ACTION is not relevant to the limitation recited in claims 2, 17 and 34. Since Table 8/7 of Edwards concerns the reference message transmitted during "continuous idle periods" it cannot be the second information blocks recited. Base claims 1, 16 and 27 recite that the second information blocks are formed by re-arranging the emulation data within the first information blocks. During the continuous idle periods no such emulation data is received to re-arrange. Accordingly, claims 2, 17 and 34 are allowable over Edwards.

Claims 37, 43 and 49 recite subject matter not anticipated by Edwards. Claims 37, 43 and 49 recite "the transmission clock rate is greater than the data processor clock rate." The OFFICE ACTION cites Edwards at column 2, lines 36 to 40 and lines 23 to 27. Edwards states at column 2, lines 36 to 40:

> "In one aspect, the trace system may be used as a rate converter for converting a transmission rate of messages transmitted to a memory system on-chip or an external system."

This teaching of converting the transmission rate is directly contrary to the recitations within respective base claims 1, 16 and 27 that "said first fixed size, said data processor clock rate, said second fixed size and said transmission clock rate related whereby a bit rate of first information blocks equals a bit rate of said second information blocks." Teaching of converting a transmission rate fails to anticipate the recited equal bit rate. Edwards states at column 2, lines 23 to 27:

> "Specifically, the trace system includes devices which operate separately from the processor, operate at internal clock speeds of the processor, or operate in modes wherein the loss of trace information does not affect processor operation."

This teaching of Edwards implies that the trace system clock and the processor internal clock operate independently. It includes no teaching that the "the transmission clock rate is greater than the data processor clock rate." Accordingly, claims 37, 43 and 49 are allowable over Edwards.

Claims 38, 44 and 50 recite subject matter not anticipated by Edwards. Claims 38, 44 and 50 recite "said second fixed size is greater in size than said first fixed size." The OFFICE ACTION cites trace buffer 227 and the size of trace messages disclosed in Tables 4 to 8 of Edwards. As pointed out above, the first fixed size of the first information blocks corresponds to the size of trace data bus 221 and the second fixed size of the second information blocks corresponds to data bus size of the output of transmission circuit 215. Edwards includes no teaching of the relative size of these busses. The intermediate data sizes such as at trace buffer 227 or FIFO 202 is not relevant to these limitations. Accordingly, claims 38, 44 and 40 are allowable over Edwards.

Claims 39, 45 and 51 recite subject matter not anticipated by Edwards. Claims 39, 45 and 51 recite "the transmission clock rate is less than the data processor clock rate." The OFFICE ACTION cites Edwards at column 8, lines 30 to 45 and at column 2, lines 36 to 40. Edwards states at column 8, lines 30 to 45:

> "Clock signal 218 may be the clock signal of processor 102 running at processor clock frequency. Signal 218 may be fed to a pre-scaler 216 circuit which determines time increments for a timestamp counter. For example, the pre-scaler may divide the processor clock frequency by an integer value, or may use the processor clock frequency value

> directly. Pre-scaler 216 provides an increment signal to a reference counter 217 which generates a reference count from a predetermined time. Reference counter 217 may provide an absolute count of time to trace processor 205 for preparing timestamp information. In one embodiment, reference counter 217 provides a 40-bit time value to trace processor 205. Trace processor 205 may in turn determine a time difference from the last trace message generated, and compress timestamp information by encoding the time difference as timestamp information in a trace message."

This teaching of Edwards is clearly directed to a time stamp counter enabling trace processor 205 to prepare "timestamp information." This portion of Edwards includes no teaching that emulation data is output at such a divided clock rate. Respective base claims 1, 16 and 27 recite that the second information blocks are output at a transmission clock rate. Claims 39, 45 and 51 recite that this transmission clock rate is less than the data processor clock rate. Thus the fact that a clock rate less than the data processor clock rate exists in Edwards is not relevant to the limitation of these claims that the transmission clock rate of output of the second information blocks is less than the data processor clock rate. Edwards states at column 2, lines 36 to 40:

> "In one aspect, the trace system may be used as a rate converter for converting a transmission rate of messages transmitted to a memory system on-chip or an external system."

This teaching of converting the transmission rate is directly contrary to the recitations within respective base claims 1, 16 and 27 that "said first fixed size, said data processor clock rate, said second fixed size and said transmission clock rate related whereby a bit rate of first information blocks equals a bit rate of said second information blocks." Accordingly, claims 39, 45 and 51 are allowable over Edwards.

Claims 30, 32 and 35 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Edwards U.S. US Patent No 6,732,307 and Teich et al U.S. Patent No. 6,229,808.

Claims 30, 32 and 35 recite subject matter not made obvious by the combination of Edwards and Teich et al. Claims 30, 32 and 35 recite "said first fixed size is an integral multiple of said second fixed size." The OFFICE ACTION states this subject matter is not disclosed in Edwards. The OFFICE ACTION cites Figure 9 and column 5, line 50 to column 6, line 21 as making obvious this subject matter. Teich et al states at column 5, lines 52 to 60:

> "The local header portion has a predetermined size. Each data portion has a predetermined size corresponding to a predetermined size of a data portion of a network packet. For example, the data portion may have a fixed size of 48 bytes corresponding to the fixed size of the data payload of an ATM cell. The overall size of the data portion of the local data packet is therefore an integer -multiple of the predetermined size of the data portion of the corresponding network packet."

This disclosure of sizes fails to make obvious the recitation of claims 30, 32 and 35 that "said first fixed size is an integral multiple of said second fixed size." The OFFICE ACTION states that the ATM cells are the first fixed size and the local data packet is the second fixed size. The only teaching in Teich et al of relative sizes is that the data payload of a network (ATM) packet is the same size as the data payload of the local data packet. Without taking into account the sizes of the ATM cell headers and the load header, this disclosure fails to require that the size of ATM cells are integral multiples of the size of the local data packet. Instead, this portion of Teich et al teaches that the size of the plural data payload portions of a local data packet is an integral multiple of the size of the data payloads of the ATM cells. This is in fact an opposite limitation to that recited in

claims 30, 32 and 35. Accordingly, claims 30, 32 and 35 are allowable over the combination of Edwards and Teich et al.

Claims 30, 32 and 35 recite further subject matter not made obvious by the combination of Edwards and Teich et al. Claims 30, 32 and 35 recite a current packet register. The Applicants respectfully submit that this structure is not disclosed in either Edwards or Teich et al. The FINAL REJECTION includes no argument that the combination of Edwards and Teich et al makes obvious this subject matter. Accordingly, claims 30, 32 and 35 are allowable over the combination of Edwards and Teich et al.

Claims 31, 33 and 36 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Edwards U.S. Patent No 6,732,307 and Baldwin et al U.S. Patent No. 5,953,339.

Claims 31, 33 and 36 recite subject matter not made obvious by the combination of Edwards and Baldwin et al. Respective base claims 1, 16 and 27 recite first information blocks having a first fixed size. The FINAL REJECTION cites LLC packets illustrated in Figure 1 of Baldwin et al as making obvious this subject matter. Baldwin et al states at column 3, lines 44 to 46:

> "AAL-2 treats the payloads from successive ATM cells from the same ATM connection as a byte stream in which variable length LLC packets are multiplexed."

This clearly states that the LLC packets are of variable length. Such a variable length does not make obvious the first fixed length recited in respective base claims 1, 16 and 27. Accordingly, claims 31, 33 and 36 are allowable over the combination of Edwards and Baldwin et al.

Claims 31, 33 and 36 recite further subject matter not made obvious by the combination of Edwards and Baldwin et al. Claim 31 recites "(a) storing a current first information block in a current packet register, (b) sequentially selecting groups of the second

fixed size bits from the current packet register as a second information block, a first selected group beginning at a next bit of said current packet register, subsequent selected groups beginning at a bit following a last bit of a prior group, until a number of bits of remaining in the current packet register is less than the second fixed number." Claims 33 and 36 similarly recite that combiner is operable to "(a) store a current first information block in a current packet register, (b) sequentially select groups of the second fixed size bits from the current packet register as a second information block, a first selected group beginning at a next bit of said current packet register, subsequent selected groups beginning at a bit following a last bit of a prior group, until a number of bits of remaining in the current packet register is less than the second fixed number." The Applicants respectfully submit that these limitations require that all bits in the second information block are derived from bits of the first information block. The FINAL REJECTION cites the ATM packets illustrated in Figure 1 of Baldwin as making obvious the claimed second information blocks. Baldwin et at states at column 3, lines 51 to 53:

> "Each ATM cell comprises an ATM header 1 (as known in the art), an STF field 2 and a plurality of LLC packets 3."

This is illustrated in Figure 1 of Baldwin et al. Thus Baldwin et al clearly teaches that ATM cells include bits not within the original LLC packets. This is contrary to the above quoted limitations of claims 31, 33 and 36. Accordingly, claims 31, 33 and 36 are allowable over the combination of Edwards and Baldwin et al.

Claims 31, 33 and 36 recite further limitations not made obvious by the combination of Edwards and Baldwin. Claims 31, 33 and 36 recite a current packet register and a last packet register.

The Applicants respectfully submit that this structure is not disclosed in either Edwards or Baldwin et al. The FINAL REJECTION includes no argument that the combination of Edwards and Baldwin et al makes obvious this subject matter. Accordingly, claims 30, 32 and 35 are allowable over the combination of Edwards and Baldwin et al.

Claim 40 to 42, 46 to 48 and 52 to 54 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Edwards U.S. Patent No. 6,732,307, Baldwin et al U.S. Patent No. 5,953,339 and Horie U.S. Patent No. 5,790,398.

Claims 40, 41, 46, 47, 52 and 53 recite subject matter not made obvious by the combination of Edwards, Baldwin et al and Horie. Claim 40 recites "said step (b) of sequentially selecting a group of the second fixed size bits and said step (e) of selecting a group of second fixed size bits stall if there is no first information block stored in either said current packet register or in said last packet register." Claims 46 and 52 similarly recite that the combiner is operable to "not sequentially select groups of the second fixed size bits (b), not select a group of second fixed size bits (e) and stall if there is no first information block stored in either said current packet register or in said last packet register." Claim 41 recites "said step (b) of sequentially selecting a group of the second fixed size bits and said step (e) of selecting a group of second fixed size bits selects a group of a second fixed size bits with a last valid first information block stored in said current packet register or in said last packet register and thereafter stalls if there is no first information block stored in either said current packet register or in said last packet register." Claims 47 and 53 similarly recite that the combiner is operable to "sequentially select a group of the second fixed size bits (b) and select a group of second fixed size bits (e) by selecting a group of a second fixed size bits with a last

valid first information block stored in said current packet register or in said last packet register and thereafter stalling if there is no first information block stored in either said current packet register or in said last packet register." Each of these claims recites conditions under which the selection of bits for the second information blocks stalls. The Applicants respectfully submit that neither Edwards, Baldwin et al nor Horie disclose such a stall. The FINAL REJECTION includes no arguments that these references make obvious this recited stall. Accordingly, claims 40, 41, 46, 47, 52 and 53 recite subject matter are allowable over the combination of Edwards, Baldwin et al and Horie.

Claims 2 to 4, 28, 42, 48 and 54 are allowable by dependence upon respective allowable base claims 1, 16 and 27.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

Texas Instruments Incorporated
P.O. Box 655474 M/S 3999
Dallas, Texas 75265
(972) 917-5290
Fax: (972) 917-4418

Respectfully submitted,

/Robert D. Marshall, Jr./
Robert D. Marshall, Jr.
Reg. No. 28,527